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10/083,714	02/26/2002	Jacques Prunier	S01022/80854	3976

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EXAMINER	
TRIMMINGS, JOHN P	

ART UNIT	PAPER NUMBER
2133	

DATE MAILED: 08/16/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/083,714	PRUNIER, JACQUES	
	Examiner	Art Unit	
	John P Trimmings	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 February 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-26* is/are rejected.

7)☒ Claim(s) *21* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *2/26/2002* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claims 1-26 are presented for examination.

Priority

The examiner acknowledges the applicant's claim of priority to 2/26/2001.

Information Disclosure Statement

The examiner has considered the applicant's Information Disclosure Statement.

Drawings

1. Figures 1, 2 and 3 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawing sheets are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

2. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference character(s) mentioned in the description: "O5 on page 3 lines 14 and 18. Corrected drawing sheets are required in reply to the Office action to avoid abandonment of the application. Any amended

replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

3. Claim 1 is objected to because of the following informalities: the phrase "capable of" in line 5 is not a positive limitation. The examiner suggests that a more definitive phrase such as "configured for" or the like be substituted in place of "capable of". Appropriate correction is required.

4. Claim 23 is objected to because of the following informalities: the phrase "scan test A method" should instead read, "A scan test method". Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claim 1 recites the limitations “the signals” in line 6, and "the other means" in the last line of the claim. There is insufficient antecedent basis for these limitations in the claim.

6. Claim 21 does not further limit Claim 16 as related to Claim 20, therefore the claim should be removed from examination pendency and cancelled (ref: 35 USC § 112 4th paragraph).

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 1-5 are rejected under 35 U.S.C. 102(a) as being anticipated by the applicant's admitted prior art (for example; page 3 line 6 of Background).

As per Claim 1:

The Background of the applicant's application teaches all of the elements of the claim, and the drawing in FIG. 3 exemplifies each element, in particular: a system for testing an integrated circuit, the integrated circuit including flip-flops (FIG.3 FF1-FF3) connected to a logic block (FIG.3 LB) and the test system (Background page 4 line 9 and FIG.3) including: test means operable for connecting the flip-flops as a register

(FIG.3 Mi), and a plurality of types of inhibition means (FIG.3 6, 2, 10), each type of inhibition means being operable for inhibiting one specific type of element of the logic block capable of disturbing the sequencing of the register (FIG.3 OD, ENI, RS) or the propagation of the signals into the logic block (for example, /ENI inhibits CK2 during /TEST), and control means for: operating the test means in synchronism with a command signal (FIG.3 TEST signal); and operating continuously the other means (all other inhibition means are also enabled with TEST signal).

As per Claim 2:

The Background of the applicant's application further teaches the integrated circuit test system of claim 1, wherein elements of a first type condition the clock signal provided to at least one flip-flop (page 3 1st paragraph and FIG.3 2).

As per Claim 3:

The Background of the applicant's application further teaches the integrated circuit test system of claim 2, wherein said elements of the first type include means for activating or inactivating said clock signal (FIG.3 TEST).

As per Claim 4:

The Background of the applicant's application further teaches the integrated circuit test system of claim 1, wherein elements of a second type condition a reset signal provided to at least one flip-flop (page 3 paragraph 2 and FIG.3 6).

As per Claim 5:

The Background of the applicant's application further teaches the integrated circuit test system of any of claim 1, wherein elements of a third type include locking

elements capable of preventing the propagation of at least one signal into the logic block (page 3 paragraph 3 and FIG.3 8).

8. Claims 16 and 24 are rejected under 35 U.S.C. 102(b) as being anticipated by Ahanin et al., U.S. Patent No. 5166604.

As per Claim 16:

Ahanin et al. teaches every aspect of the applicant's claim in column 4 lines 48-68 and column 5 lines 1-11.

As per Claim 24:

Ahanin et al.further teaches a scan test method as defined in claim 16, wherein performing a scan test of the selected disturbing element comprises inhibiting the selected disturbing element to load a test vector into the flip-flops and enabling the selected disturbing element to observe operation of the logic block in response to the test vector (column 5 lines 1-11.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 6, 7, and 11-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over the applicant's admitted prior art, in view of Ahanin et al., U.S. Patent No. 5166604.

As per Claim 6:

The Background of the applicant's application teaches scan test circuitry in an integrated circuit having a logic block (FIG.3 LB) including elements capable of disturbing a scan test (FIG.3 OD, ENI, RS), comprising: a plurality of flip-flops operable as a register in a scan test mode (FIG.3 FF1-FF3); inhibiting circuits for inhibiting each of the disturbing elements of the logic block from disturbing a scan test (FIG.3 10, 2, 6). But the prior art reference fails to specify a controller for controlling the TEST signal of fig.3. However, in an analogous art, Ahanin et al. teaches a controller (FIG.3) for individually controlling each of the inhibiting circuits during a scan test (column 3 lines 63-68 and column 4 lines 1-41). And in column 1 lines 5-31, the inventor boasts of a way to test asynchronous test set/reset signals during scan test. One with ordinary skill in the art at the time of the invention, motivated as suggested by Ahanin et al., would add the controller of that invention to the circuit described in the applicant's prior art in order to control a plurality of inhibit gates.

As per Claim 7:

Ahanin et al. further teaches the scan test circuitry as defined in claim 6, wherein the controller is configured to load into the flip-flops, with all disturbing elements inhibited (column 4 lines 48-63), a test vector for testing a first disturbing element (column 4 lines 65, for example, NPRESET) and, subsequently, to enable the first disturbing element and to observe operation of the logic block in response to the test vector (column 4 lines 64-68 and column 5 lines 1-11). And in view of the motivation previously stated, the claim is rejected.

As per Claim 11:

Ahanin et al. further teaches the scan test circuitry as defined in claim 6, wherein the controller is further configured to perform a scan test with all disturbing elements inhibited by the respective inhibiting circuits (column 4 lines 4-41). And in view of the motivation previously stated, the claim is rejected.

As per Claim 12:

The Background of the applicant's application further teaches the scan test circuitry as defined in claim 6, wherein at least one of the inhibiting circuits is configured to inhibit a disturbing element that affects a clock signal supplied to at least one of the flip-flops (FIG.3 2). And in view of the motivation previously stated, the claim is rejected.

As per Claim 13:

The Background of the applicant's application further teaches the scan test circuitry as defined in claim 6, wherein at least one of the inhibiting circuits is configured to inhibit a disturbing element that affects a reset signal supplied to at least one of the flip-flops (FIG.3 6). And in view of the motivation previously stated, the claim is rejected.

As per Claim 14:

The Background of the applicant's application further teaches the scan test circuitry as defined in claim 6, wherein at least one of the inhibiting circuits is configured to inhibit a disturbing element that affects at least one input from the scan test circuitry to the logic block. Any one of the circuit (FIG.3 10, 2, 6) will alter the state of any flip-flop (FF1-FF3), which in turn affects the Qi outputs and thus each Ii input to the logic block. And in view of the motivation previously stated, the claim is rejected.

As per Claim 15:

The Background of the applicant's application further teaches the scan test circuitry as defined in claim 6, wherein at least one of the inhibiting circuits is configured to inhibit a disturbing element that affects at least one output of the logic block to the scan test circuitry (FIG.3 10). And in view of the motivation previously stated, the claim is rejected.

10. Claims 8-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over the applicant's admitted prior art, in view of Ahanin et al., U.S. Patent No. 5166604 as applied to Claim 6, and further in view of Nadeau-Dostie et al., U.S. Patent No. 6510534. The circuitry of Claim 6 fails to teach that the disturbing elements are tested in an inactive and an active state. However, in an analogous art, Nadeau-Dostie et al. teach this feature where column 12 lines 20-49 specify each of the claimed test modes. And in column 3 lines 7-30, the inventor recites the advantage of testing non-scanable elements in the logic by initializing the elements both as active and as inactive and then scanning the results. One with ordinary skill in the art at the time of the invention, motivated by Nadeau-Dostie et al. as suggested, would add the capability of Nadeau-Dostie et al. to the circuit of Claim 6 in order to fully test the inaccessible internal logic of a circuit.

11. Claims 17 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ahanin et al., U.S. Patent No. 5166604 as applied to Claim 16, and further in view of Nadeau-Dostie et al., U.S. Patent No. 6510534. The methodology of Claim 16 fails to teach that the disturbing elements are tested in an inactive and an active state.

However, in an analogous art, Nadeau-Dostie et al. teach this feature where column 12 lines 20-49 specify each of the claimed test modes. And in column 3 lines 7-30, the inventor recites the advantage of testing non-scanable elements in the logic by initializing the elements both as active and as inactive and then scanning the results. One with ordinary skill in the art at the time of the invention, motivated by Nadeau-Dostie et al. as suggested, would add the capability of Nadeau-Dostie et al. to the circuit of Claim 6 in order to fully test the inaccessible internal logic of a circuit.

12. Claims 19-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ahanin et al., U.S. Patent No. 5166604 as applied to Claim 16, and in view of the applicant's admitted prior art.

As per Claim 19:

The scan test method as defined in claim 16 fails to further limit the method wherein inhibiting all of the disturbing elements except a selected disturbing element comprises inhibiting at least one disturbing element that affects a clock signal supplied to at least one of the flip-flops. However, the prior art reference does teach this feature in FIG.3 2, and page 3 paragraph 1. And in view of the motivation previously stated, the claim is rejected.

As per Claim 20 and 21:

The scan test method as defined in claim 16 fails to further limit the method wherein inhibiting all of the disturbing elements except a selected disturbing element comprises inhibiting at least one disturbing element that affects a reset signal supplied to at least one of the flip-flops. However, the prior art reference does teach this feature

in FIG.3 6, and page 3 paragraph 2. And in view of the motivation previously stated, the claim is rejected.

As per Claim 22:

The scan test method as defined in claim 16 fails to further limit the method wherein inhibiting all of the disturbing elements except a selected disturbing element comprises inhibiting at least one disturbing element that affects an input to the logic block from at least one of the flip-flops. Any one of the circuits (FIG.3 10, 2, 6) will alter the state of any flip-flop (FF1-FF3), which in turn affects the Qi outputs and thus each Ii input to the logic block. And in view of the motivation previously stated, the claim is rejected.

As per Claim 23:

The scan test method as defined in claim 16 fails to further limit the method wherein inhibiting all of the disturbing elements except a selected disturbing element comprises inhibiting at least one disturbing element that affects an output of the logic block to at least one of the flip-flops. However, the prior art reference does teach this feature in FIG.3 10, and page 3 paragraph 3. And in view of the motivation previously stated, the claim is rejected.

13. Claims 25 and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ahanin et al., U.S. Patent No. 5166604 as applied to Claim 16, and in view of Nadeau-Dostie et al., U.S. Patent No. 6510534. The methodology of Claim 16 fails to teach that the disturbing elements are tested in an inactive and an active state. However, in an analogous art, Nadeau-Dostie et al. teach this feature where column 12

lines 20-49 specify each of the claimed test modes. And in column 3 lines 7-30, the inventor recites the advantage of testing non-scanable elements in the logic by initializing the elements both as active and as inactive and then scanning the results. One with ordinary skill in the art at the time of the invention, motivated by Nadeau-Dostie et al. as suggested, would add the capability of Nadeau-Dostie et al. to the method of Claim 16 in order to fully test the inaccessible internal logic of a circuit.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John P Trimmings whose telephone number is 703-305-0714. The examiner can normally be reached on Monday through Thursday, 7:30 AM to 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert DeCady can be reached on 703-305-9595. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

John P Trimmings
Examiner
Art Unit 2133

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GUY J. LAMARRE
PRIMARY EXAMINER